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322454(22)

B. E. (Fourth Semester) Examination, Nov.-Dec. 2021

(New Scheme)

(CSE Branch)

COMPUTER SYSTEMS ARCHITECTURE

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) in each unit is compulsory. Attempt any* ***two*** *from (b), (c) and (d). Part (a) is of 2 marks and part (b), (c) and (d) are of 7 marks each.*

Unit-I

1. (a) What do you mean by Micro Routine? 2

(b) Explain various types of computer instruction formats. A two-word instruction is stored in memory at an address designated by symbol W. The address field of the instruction (stored at $W + 1$) is designated by symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index Register contains the value X. State how Z is calculate from the other addresses if the addressing mode of the instruction is : 7

(i) Direct

(ii) Indirect

(iii) Relative

(iv) Indexed

(c) Differentiate between hardwired control unit and micro-programmed control unit. 7

(d) Explain the working of a typical Micro-programmed control unit with a neat diagram. 7

Unit-II

2. (a) What is divide overflow? 2

(b) Show the contents of Registers E, A, Q and SC during the process of division of 10100011 by 1011 using Restoring method. 7

(c) Show step-by-step Multiplication Process using Booth Algorithm. Assume 5 bit registers that hold signed numbers are $(+15) \times (-13)$. 7

(d) Explain Fast adders in detail. 7

Unit-III

3. (a) Write the memory hierarchy. 2

(b) A two way set associative cache memory uses blocks of four words. The cache can accommodate a table of 2048 words from main memory. The main memory size is 128 K × 32.

(i) Formulate all pertinent information required to construct the cache memory.

(ii) What is the size of cache memory? 7

(c) The access time of cache memory is 100 ns and that of main memory 1000 ns. It is estimated that

80% of the memory request for read and remaining 20% for write. The hit ratio for read access only 0·9. A write through procedure is used.

(i) What is the average access time of the system considering only memory read cycle?

(ii) What is the average access time of the system for both read and write required?

(iii) What is the hit ratio taking into consideration the wirte cycles? 7

(d) Explain the working of an Associative Memory with neat diagram. 7

Unit-IV

4. (a) What are Interrupts? 2

(b) Explain the working of Direct Memory Access with a neat diagram. 7

(c) Differentiate between Synchronous and Asynchronous data transfer. 7

(d) Explain programmed I/O with example. 7

Unit-V

5. (a) Define data dependency. 2

(b) Explain Flynn's classification of parallel architecture. 7

(c) What do you understand by pipelining? Differentiate between instruction pipeline and arithmetic pipeline. 7

(d) A non pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? 7